REMARKS

Claims 6, 10, 15 and 16 are pending. Claims 11 and 12 are canceled without prejudice or disclaimer, and claim 10 is amended. A marked-up version showing the changes made to claim 10 is attached hereto as "**Version with markings to show changes made**."

Claim 12 was objected to under 37 CFR §1.75(c). The objection has been rendered moot by cancellation thereof.

Claims 10-12 were rejected under 35 USC §102(e) as being anticipated by Pan. Favorable reconsideration of this rejection is respectfully requested.

Claim 10 has been amended to incorporate the features of claim 11, and to clarify that said N atoms do not reach said substrate. See Fig. 7C and the first paragraph on page 14 of the specification.

In the case of ion implantation of nitrogen atoms into a silicon substrate, the penetration depth of the nitrogen atoms becomes: about 2.3nm in the case the acceleration voltage of 1kV is used; about 23nm in the case the acceleration voltage of 10keV is used; about 230nm in the case the acceleration voltage of 100keV is used; and about 2 microns in the case the acceleration voltage of 1000keV is used.

Thus, in the ordinary case of a gate oxide film having the thickness of 1-10nm, an acceleration voltage of 5keV or less is preferable. On the other hand, taking into consideration the effect of the thermal annealing process that follows the ion implantation process, the preferable range

of the ion implantation energy would be 10 keV or less, in conformity with amended claim 10.

With respect to Pan, it is submitted that this reference achieves "hardening" of the semiconductor/oxide interface. See column 1, lines 41 or column 3, line 42 of Pan. Thus, it is believed that the nitrogen atoms implanted according to the process of Pan inherently reach the semiconductor/oxide interface. Further, Pan is entirely silent about the feature of implanting the nitrogen atoms such that the nitrogen atoms to not reach the substrate. In fact, Fig 1b of Pan shows, although schematically, that the hardened gate oxide layers 14a extend from the bottom interface to the silicon substrate up to the top surface thereof.

While Pan teaches the use of ion implantation energy of 100keV or less, it is believed that the reference does not teach the ion implantation process of nitrogen conducted such that the nitrogen atoms do not reach the substrate as set forth in amended claim 10.

Claims 6, 15 and 16 have been allowed.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by Applicants would be desirable to place the application in better condition for allowance, the Examiner is encouraged to telephone Applicants' undersigned attorney.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/428,052

IN THE CLAIMS:

Claim 10 has been amended as follows:

10. (Seven Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate by a thermal oxide film;

forming a gate electrode pattern on said gate oxide film such that said gate electrode pattern is in direct contact with said gate oxide film;

forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms, after said step of introducing said impurity element, into said gate oxide film while using said gate electrode pattern as a mask, such that said N atoms do not reach said substrate,

wherein said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions conducted under an acceleration voltage not exceeding 10keV, with a dose of $1 - 3 \times 10^{14}cm^{-2}$.